Advances in large-area microelectronic device deprocessing for physical failure analyses and quality control

Pawel Nowakowski, Michael Boccabella, Mary Ray, Paul Fischione
E.A. Fischione Instruments, Export, PA, USA
p_nowakowski@fischione.com

Introduction

The rapidly growing semiconductor manufacturing sector reported sales nearing $400 billion in 2017, which was a 16% increase over 2015 [1, 2]. High-volume semiconductor device manufacturing requires robust quality control and failure analyses processes. Many failure analysis techniques, both nondestructive and destructive, have been developed in the past five decades [3-6]. A popular technique is device delayering, which is the controlled removal of device layers from the top-down. Information gained through this technique can support quality control and failure analyses efforts, as well as yield product and process improvement data. Focused ion beam (FIB) techniques are often used when delayering semiconductor devices [5, 7, 8]. However, using FIB technology for device delayering has limitations; the most important limitation being the relatively small delayering area: about 20 x 20 µm for Ga FIB [5] and about 100 x 100 µm for Xe FIB [8-10]. That limitation prevents the exposure of a large slope area on the sample, which reveals all layers simultaneously. Tools that yield a small delayering area not only limit characterization, they also limit sample size. For example, FIB-based techniques cannot currently sample multiple regions of interest (ROI) on a whole (unbroken) 300 mm wafer.

The delayering process is complex and requires prior process knowledge, such as cross-section architecture, composition, and layer uniformity. One can distinguish two strategies for microelectronic device deprocessing:

- **Spot milling** down to substrate (silicon) followed by scanning electron microscope (SEM) observation of the resulting slope area, which exposes all layers of the device simultaneously.

- **Layer-by-layer milling** (top-down delayering) of device material with iterative SEM observation.

In this paper we discuss advances in semiconductor device deprocessing for product development, failure analysis, and quality control using low-energy, argon broad ion beam (BIB) milling. A unique, automated technique for Ar BIB milling of whole 300 mm wafers is contrasted with tabletop Ar BIB milling of 300 mm wafer pieces.

Experiment

An instrument designed for pre-CD-SEM sample preparation, the WaferMill™ ion beam delayering solution [Fischione Instruments], was used for spot milling of a whole 300 mm wafer. The instrument is fully automated and has a front-opening unified pod (FOUP) loading station that holds up to 25 wafers, a four-axis wafer handling robot that loads and unloads wafers to the process chamber, and a controller unit with a user interface.

The process chamber hosts a linear stage, which can move a wafer in x and y directions with 5 µm accuracy. The stage is equipped with an electrostatic chuck that grips the wafer in place to provide a uniform milling plane by eliminating wafer bow. The wafer presence sensors indicate when a wafer is in the process chamber. The process chamber is fitted with a turret with three Ar ion sources. The turret allows rocking ± 175°. The three Ar ion sources are arranged in a circle and spaced 120° apart. Each source is positioned 22.5° from the horizontal plane. This geometrical arrangement allows fast and uniform milling. The acceleration voltage is variable from 0.1 to 6 keV. The ion beam diameter and current are also user adjustable. Following milling, in situ viewing is provided by a digital camera with 15 mm (low magnification) and 1.4 mm (high magnification) fields of view.

A tabletop BIB mill, the SEM Mill [Fischione Instruments], was used to delayer wafer pieces. This ion mill is fitted with two Ar ion sources with adjustable beam angles (0 to 10°), beam energy (0.1 to 10 keV), and beam diameter/current (0.5 to 5 mm). The maximum sample dimensions are 32 x 25 mm. In situ viewing allows observation during delayering at up to 1,960X magnification.

For imaging of delayered devices, a Scios DualBeam SEM [Thermo Fisher Scientific] was used. Energy dispersion spectroscopy (EDS) analysis was accomplished with the X-Max 150 detector [Oxford Instruments].

The wafer used in the experiment was issued from a production line and contained both logic and memory.

Results and Discussion

Spot milling of a whole 300 mm wafer

Five locations (spots) on the wafer were selected for milling. Because redeposition of milled material from one spot to another is a concern with ion milling in general, some of the spots selected were in close proximity to other spots (Figure 1). The milling times were varied: spot 1, 15 min.; spot 2, 2 min.; spot 3, 4 min.; spot 4, 6 min.; and spot 5, 25 min. All spots were Ar ion milled at 6 keV.
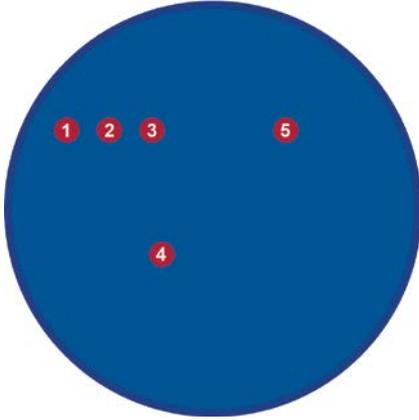

Figure 1: Position of milling spots on a 300 mm wafer.

The distance between spots 1, 2, and 3 was 25 mm, between spot 3 and 4 was 50 mm, and between spot 3 and 5 was 75 mm. Table 1 summarizes the milling locations, proximity to neighboring milling locations, milling times, and the diameter of the wafer area affected by the Ar ion beams (which is observable by the naked eye). Figure 2 shows SEM and EDS analyses of the area between spot 1 and 2. No redeposition between or within the milling spots was observed.

Table 1: Milling time and beam affected area (diameter) for all investigated spots.

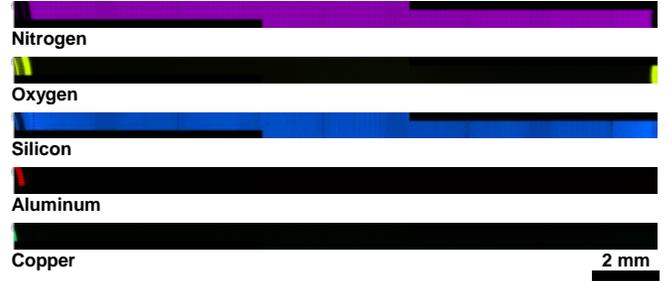| Spot number	Distance from the nearest neighbor [mm]	Milling time [min.]	Diameter of beam-affected area [mm]
1	25	15	14
2	25	2	10.8
3	25	4	11.8
4	50	6	12.8
5	75	25	17.8

Figure 2: EDS element maps collected at 5 keV show space between two milling spots (1 and 3, Figure 1) milled at 6 keV with an Ar ion beam (WaferMill system). Only Si_3N_4 was detected between the processed spots, which is the top layer of the investigated 300 mm wafer.

Figure 3 presents a spot milled down to the silicon substrate; beam energy was 6 keV for 25 min. Part of a large slope that exposes all device layers is shown. Figure 4 shows a higher magnification image of a slope exposed by Ar ion milling. Using the spot milling approach, a large area can be investigated for quality control or failure analysis purposes.
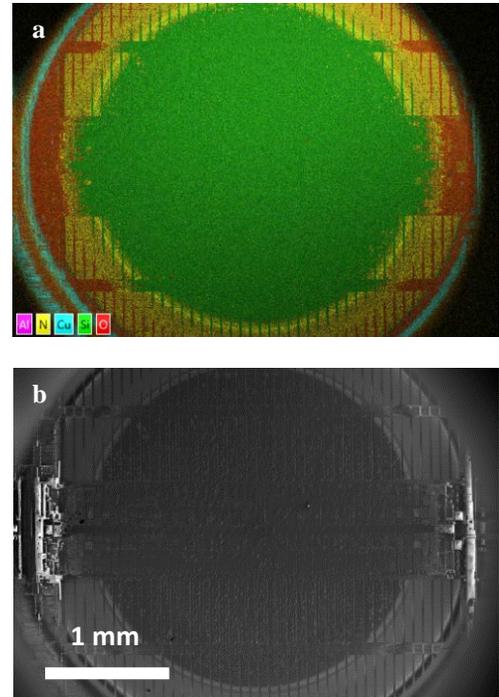

Figure 3: Milling spot 5 processed at 6 keV for 25 min. EDS layered element maps (a) and secondary electron SEM contrast image (b) are shown.

An example of a large (800 µm) slope area is shown in Figure 4a. Figure 4b represents a zoom-in of one memory division and Figure 4c shows high magnification of memory cells. Taking into account the EDS data collected at 5 kV acceleration voltage (Figure 4d-h), one can distinguish six layers. From top to bottom, the layers are: Cu metal line; W metal line, SiO_2 passivation layer; memory cells consisting of Zr, SiO_2, and Si_3N_4; W metal line; memory cells; and W metal line and Si substrate.

(a) Large (800 µm slope area)

(b) Memory area

(c) Memory cells

(d) Copper L series

(e) Tungsten M series

(f) Oxygen K series

(g) Zirconium L series
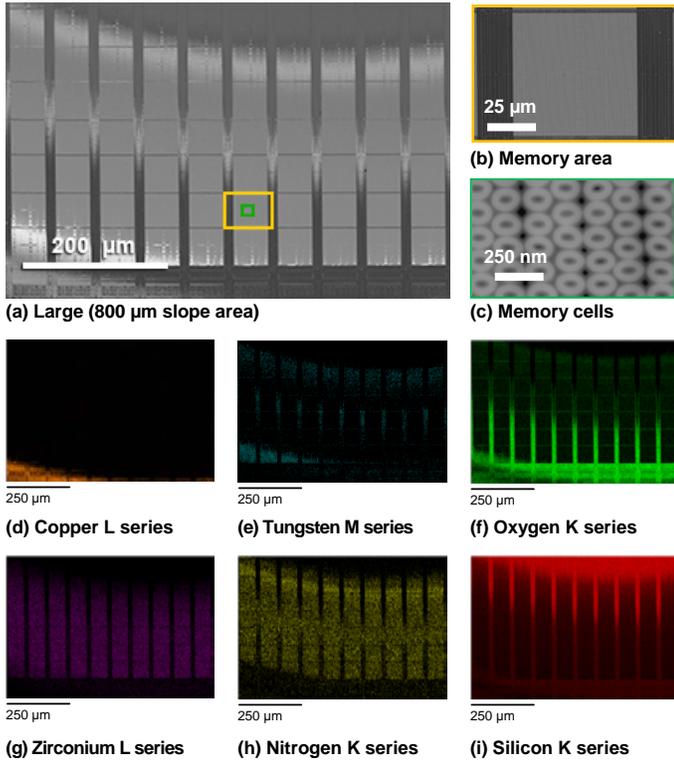
(h) Nitrogen K series

(i) Silicon K series

Figure 4: A large slope area from spot 5 with all device layers exposed. Shown are a backscattered electron (BSE) SEM contrast image of the memory area of the device with an 800 µm field of view (a); a magnification image of the memory area (b); a high-magnification image of memory cells (c); and EDS maps of copper, tungsten, oxygen, zirconium, nitrogen, and silicon (d-i).

Another approach to microelectronic device deprocessing is removing device material one layer at a time or removing layers until a desired depth is reached. In this example, V-NAND 3D flash memory was milled at 4 kV using the WaferMill system. The BIB milling process was stopped when the memory portion of the device was uncovered. Figure 5, shows SEM images of the delayered area at different magnifications. The homogenous surface obtained from BIB milling allowed detailed observation and characterization of the memory cells. A detailed report of delayering V-NAND 3D flash memory was published by the authors in [11].
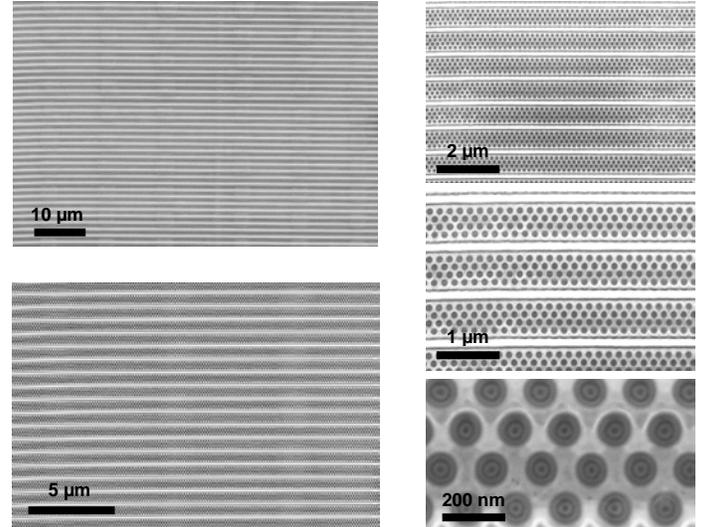

Figure 5: BSE SEM images of top down delayering of 3D V-NAND flash memory. Images show clean, large areas after Ar BIB milling at 4 keV.

Top-down delayering of wafer pieces

The sample used in this experiment was a 5 x 10 mm solid-state drive (SSD) containing air gap structures. First, a cross-section sample was prepared to serve as a reference during the delayering process. The cross-section sample was prepared by applying a protective mask to create a cross-section configuration and then milled in the SEM Mill. From the cross section (Figure 6), one can identify the device layers, composition, and uniformity; the cross-section investigation shows that the air gaps are rhombohedric in shape and EDS reveals that they have a Si_3N_4 and W composition.

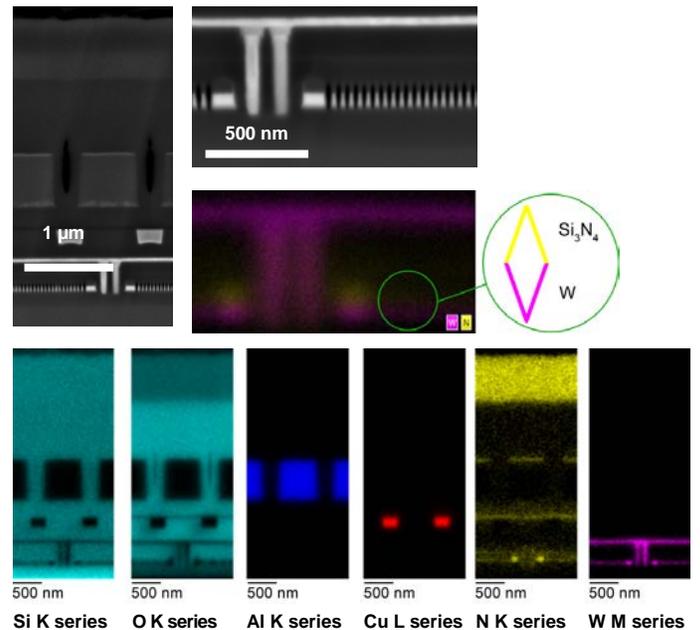Si K series O K series Al K series Cu L series N K series W M series

Figure 6: Clockwise from top left. SSD cross-section sample after Ar BIB milling at 5 keV; magnified image of cross-section sample; air gap's rhombohedric shape; EDS measurements of the air gap.

The delayering process was carried out from the top-down, using 5 keV Ar BIB and 3° milling angle with 360° continuous stage rotation. Two delayering strategies were employed when investigating the air gap structures:

- Mill down to the substrate, followed by observation of the **slope** area by SEM.

- Remove device material layer-by-layer to reach the desired level of investigation.

Slope observation. Figure 7 shows an area across the air gap architecture, from the top rich in Si_3N_4 to the bottom rich in W. EDS analyses highlight that no redeposition accrued over the large slope area uncovered by the Ar BIB milling process.
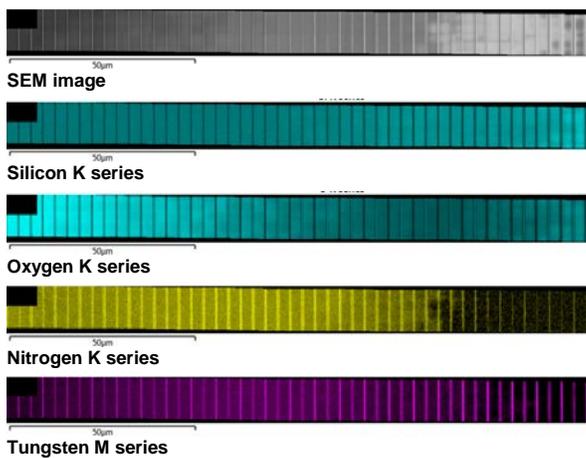

SEM image

Silicon K series

Oxygen K series

Nitrogen K series

Tungsten M series

Figure 7: Large, clean area across air gap architecture, from the top rich in Si_3N_4 to the bottom rich in W.

Once the device was milled down to the silicon substrate, detailed investigation was possible. The EDS analyses shown in Figures 8-9 confirm no redeposition and an extremely clean surface following Ar BIB milling. The SEM images highlight the quality of the delayered area's surface, which allowed detailed observation and measurements.
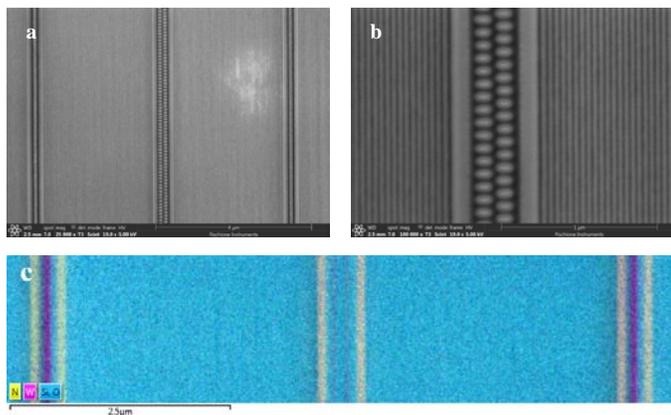

Figure 8: Detailed observation of the top portion of the air gap structure. SEM images (a, b) taken at different magnifications; EDS analyses (c) at 5 keV.
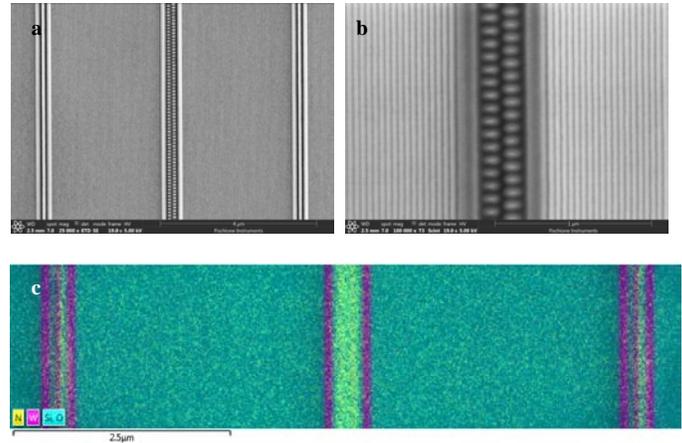

Figure 9: Detailed observation of the bottom portion of the air gap structure. SEM images (a, b) taken at different magnifications; EDS analyses (c) at 5 keV.

Layer-by-layer observation

In this example, we chose to stop milling at the copper metal line of the SSD device (see the cross-section image in Figure 6). Figure 10a shows a low-magnification SEM image and Figures 10b-f show the EDS analyses of the sample after BIB milling. EDS data were collected at 5 keV. Figure 11 shows high-magnification images of the delayered area at the copper line level. A large, 400 µm uniform area can be observed. The investigation at high magnification confirms uniformity of copper metal lines obtained after Ar BIB milling. The BSE contrast image shown in Figure 11a was taken in the center of the field of view of Figure 10a.
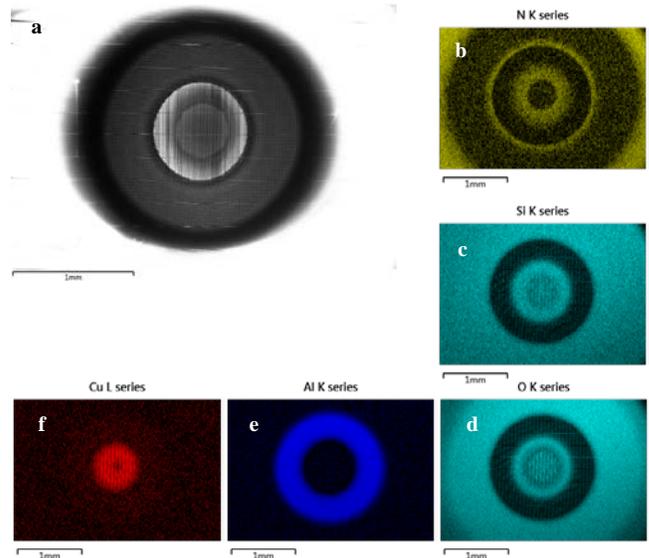

Figure 10: SEM image (a) of a SSD device delayered down to the copper line and EDS analyses (b-f) at 5 keV.
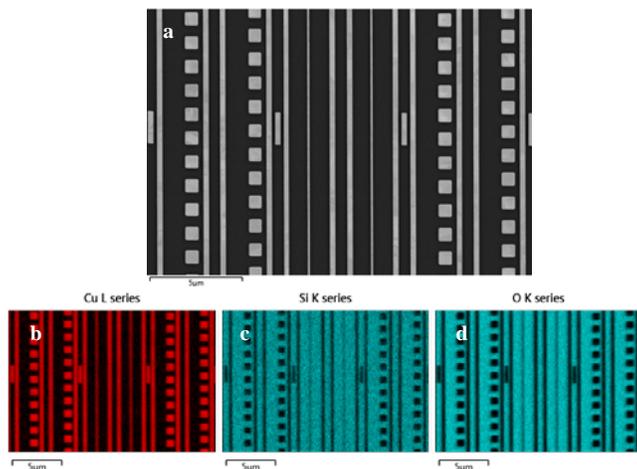
Figure 11: High-magnification SEM image (a) of a SSD device delayered down to the copper line and EDS analyses (b-c) at 5 keV.

Conclusions

Ar BIB milling is a practical solution for accurate delayering of advanced microelectronic devices. Successful device delayering can be achieved by either:

- **Spot milling** down to substrate (silicon) followed by SEM observation of the slope area, which exposes all layers of the device simultaneously.

- **Layer-by-layer milling** (top-down delayering) of device material with iterative SEM observation.

These two strategies are easily achieved – for either small wafer pieces (up to 30 mm diameter) or full 300 mm wafer investigation. No redeposition is observed between the milled spots or within a milled spot.

A large uniform area significantly greater than 100 x 100 µm can be achieved by the described techniques.

Ar BIB milling reveals the complex architectures of microelectronic structures and permits accurate targeting of specific layers for failure analyses and quality control.

In the described technique, the initial flatness of the wafer surface is critical for uniform semiconductor device delayering. Significant surface topography may require an adjustment of milling parameters. This is especially true for fully fabricated wafers, where the final aluminum pads and lines are significantly elevated from the surrounding areas. For these cases, the delayering strategy must be adapted to meet the investigator's goals. A detailed description of specific delayering strategies for wafers with significant surface topography exceeds the scope of this investigation, but will be investigated in the future.

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